UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,310	09/11/2003	Richard L. Coulson	ITL.1029US (P16765)	5388

21906	7590	11/02/2006	

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EXAMINER
BHAT, ADITYA S

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/660,310	COULSON ET AL.
	Examiner	Art Unit	
	Aditya S. Bhat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>11 September 2006</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-42</u> is/are pending in the application.

  4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-9,11-19 and 21-42</u> is/are rejected.

7)☒ Claim(s) <u>10 and 20</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>11 September 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  a)☐ All b)☐ Some * c)☐ None of:

  1.☐ Certified copies of the priority documents have been received.

  2.☐ Certified copies of the priority documents have been received in Application No. _____.

  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
  Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9,11-19, and 21-42 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Giovannetti (USPN 5,815,648).

With regards to claims 1 and 13, Giovannetti (USPN 5,815,648) teaches a method comprising, or an article comprising a medium storing instructions that, if executed, enable a processor based system to

monitoring a temperature; (Col. 4, lines 35-40) and

in response to a detection of a temperature condition, transitioning the cache memory(Col. 4, lines 35-43) (figure 4) from a write-back cache to a write through cache (Col. 5, lines 9-10) (Col.2, lines 2-4)(Col. 6, lines 24-25)

With regards to claims 2, 14, 27 and 41, Giovannetti (USPN 5,815,648) teaches monitoring the temperature (Col. 4, lines 35-40) of a ferroelectric polymer cache memory. (Col. 1, lines 53-55)

With regards to claim 3, Giovannetti (USPN 5,815,648) teaches adjusting the operation of a system using said memory at a first temperature and, in response to the

detection of a higher, second temperature, transitioning the cache from a write-back

cache to a write-through cache. (Col. 4, lines 35-43) (Col. 5, lines 9-10)

With regards to claim 4, Giovannetti (USPN 5,815,648) teaches slowing an

operation of said system at said first temperature. (Col. 4, lines 55-67)

With regards to claim 5, Giovannetti (USPN 5,815,648) teaches reducing pre-

fetching at said first temperature. (Col. 4, lines 55-67)

With regards to claim 6, Giovannetti (USPN 5,815,648) teaches adjusting what

data is cached based on a detection of said first temperature. (Col. 4, lines 39-46)

With regards to claim 7 and 16, Giovannetti (USPN 5,815,648) teaches shutting

off the said cache memory at a temperature above said second temperature. (Col. 5,

lines 9-10)

With regards to claim 8, Giovannetti (USPN 5,815,648) teaches monitoring for a

temperature lower than said second temperature. (Col. 4, lines 35-43)

With regards to claim 9, Giovannetti (USPN 5,815,648) teaches upon detecting a

lower temperature, resuming operation of said cache memory. (Col. 4, lines 35-43)

With regards to claims 11 and 21, Giovannetti (USPN 5,815,648) teaches a

processor-based system to shut off the cache and invalidate all the cache lines. (Col. 5,

lines 9-10)

With regards to claims 12 and 17, Giovannetti (USPN 5,815,648) teaches

flushing a cache line in said cache memory that has not been written through to a

source memory. (Col. 2, lines 36-39)

With regards to claim 15, Giovannetti (USPN 5,815,648) teaches storing instructions that, if executed, enable a processor-based system to adjust the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transition the cache memory from a write-back to a write-through cache. (Col. 4, lines 35-43) (Col. 5, lines 9-10)

With regards to claim 18, Giovannetti (USPN 5,815,648) teaches a processor-based system to monitor for a temperature lower than said second temperature. (Col. 4, lines 39-43)

With regards to claim 19, Giovannetti (USPN 5,815,648) teaches a processor-based system to resume operation of said cache memory upon detecting a lower temperature. (Col. 4, lines 35-43)

With regards to claim 26, Giovannetti (USPN 5,815,648) teaches a processor-based system comprising:

a processor; (110;figure 1)

a disk drive coupled to said processor; (15;figure 1)

a cache memory coupled said processor; (140;figure 1) and

a storage(100;figure 1) to store a cache driver to monitor a temperature and in response to the detection of a temperature condition, (Col. 4, lines 35-43) transition the cache memory from write-back cache to a write through cache memory. (Col. 5, lines 9-11) (figure 4)

With regards to claim 28, Giovannetti (USPN 5,815,648) teaches the cache memory is a flash memory. (140;figure 1)

With regards to claim 29, Giovannetti (USPN 5,815,648) teaches storing instructions that enable a dirty line to be flushed. (Col. 2, lines 36-39)

With regards to claim 30, Giovannetti (USPN 5,815,648) teaches instructions that enable the system to adjust for reduced speed operation at a first temperature, switch to a write-through cache memory at a second higher temperature, and invalidate cache lines and shut off the cache memory at still a higher temperature. (Col. 5, lines 9-10) (Col.2, lines 2-4)(Col. 6, lines 24-25)

With regards to claim 31, Giovannetti (USPN 5,815,648) teaches storing instructions that enable the cache memory to return to full speed operation. (Col. 5, lines 9-10)

With regards to claim 32, Giovannetti (USPN 5,815,648) teaches stores instructions that enable the system to wait for reduced speed temperature range to resume cache operations after shutting off the cache memory in response to a temperature condition. (Col. 5, lines 9-10) (Col.2, lines 2-4)(Col. 6, lines 24-25)(Col. 4, lines 39-41)

With regards to claim 33, Giovannetti (USPN 5,815,648) teaches instructions that enable the system to resume cache operations after shutting off the cache memory in response to a cache condition by initially resuming reduced speed operations in a first stage and thereafter resuming normal operations. (Col. 5, lines 9-10) (Col.2, lines 2-4)(Col. 6, lines 24-25)(Col. 4, lines 39-41)

With regards to claims 34 and 42, Giovannetti (USPN 5,815,648) teaches a cache memory includes a temperature sensor. (Col. 4, lines 35-39)

With regards to claim 35, Giovannetti (USPN 5,815,648) teaches a component to receive an indication of a temperature of a cache memory (col. 4, lines 39-41)

With regards to claim 36, Giovannetti (USPN 5,815,648) teaches a component to vary the operation of a system to adjust for the temperature-affected operation of said cache memory. (Col. 5, lines 9-10) (Col.2, lines 2-4)(Col. 6, lines 24-25)(Col. 4, lines 39-41)

With regards to claim 37, Giovannetti (USPN 5,815,648) teaches a component to adjust a caching operation of the system in response to a temperature indication from said memory. (Col. 5, lines 9-10) (Col.2, lines 2-4)(Col. 6, lines 24-25)(Col. 4, lines 39-41)

With regards to claim 38-39, Giovannetti (USPN 5,815,648) teaches a component to shut off said cache in response to a temperature indication. (Col. 5, lines 9-10)

With regards to claim 40, Giovannetti (USPN 5,815,648) teaches a cache memory (140; figure 1)

Allowable Subject Matter

2.   The following is a statement of reasons for the indication of allowable subject matter: Claims 10 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 10 & 20:

The primary reason for the allowance of claims 10 and 20 is the inclusion of the method steps of: waiting for a power cycle before resuming cache operations. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3.   Applicant's arguments with respect to claims 1-42 have been considered but are moot in view of the new ground(s) of rejection. .

Conclusion

4.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sachs et al (USPN 5,091,846) teaches Cache providing caching/non-caching write-through and copyback modes for virtual addresses and including bus snooping to maintain coherency, Stamm et al. (USPN 5,155,843) teaches a error transition mode for multi-processor system, and Somani et al. (USPN 5,524,212) teaches a multiprocessor system with write generate method for updating cache.
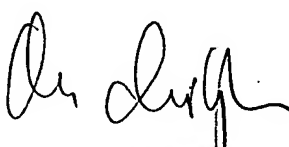
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can

be reached on 571-272-2269. The fax phone number for the organization where this

application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat
October 24, 2006

MICHAEL NGHIEM
PRIMARY EXAMINER